LISTING OF CLAIMS:

1-11. **(canceled)**

12. **(original)** An input/output (I/O) device for use in a process control system for communications in a process control network, the process control system including a plurality of I/O devices in communication using a bus, the I/O device comprising:

an interface for communicatively linking the I/O device with the bus; and

a device processor coupled with the interface for controlling operation of the device including performing fault detection for the device;

wherein the device processor, upon detection of a potential device fault, severs the communication link provided by the interface with the bus.

13. **(original)** The I/O device of claim 12 wherein the bus includes a data line and the interface communicatively links the I/O device with the data line of the bus, and wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the interface with the data line.

14. **(original)** The I/O device of claim 13 wherein the I/O device further comprises a relay device coupled between the device processor and the data line of the bus, the relay having a first state communicatively linking the I/O device with the data line, and a second state severing the communicative link between the I/O device and the data line of the bus, wherein the device processor, upon detection of the potential device fault, severs the communication link with the bus by actuating the relay to the second state.

15. **(original)** The I/O device of claim 13 wherein the data line of the bus is a data line capable of being affected by the I/O device.

16. **(original)** The I/O device of claim 15 wherein the data line of the bus is at least one of a transmit data line and clock data line.

17. **(original)** The I/O device of claim 13 and further comprising a driver device coupled between the device processor and the interface, the driver device having a driver output coupled to the interface and readable by the processor, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the interface with the data line, performs further fault detection on the device by forcing states to the driver output, and determines a device fault responsive to readings from the driver output.

18. **(original)** The I/O device of claim 12 wherein the bus includes a plurality of data lines, and the interface communicatively links the I/O device to the plurality of data lines, wherein the device processor, upon detection of the potential device fault, severs the communication link provided by the interface with the plurality of data lines of the bus.

19. **(original)** The I/O device of claim 12 wherein the fault detection is an initial fault detection, and further comprising a later fault detection performed by the I/O device after the communicative link from the I/O device and the bus is severed.

20. **(original)** The I/O device of claim 19 wherein the later fault detection is performed in a similar manner to the initial fault detection.

21. **(original)** The I/O device of claim 12 wherein the potential device fault includes the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus, and the device processors severing of the communication link with the bus allows the other I/O devices to communicate to one another over the bus.

22. **(original)** The I/O device of claim 21 wherein the bus includes at least one data line and the interface communicatively links the I/O device with the at least one data line of the bus, and the I/O device prohibiting other I/O devices utilizing the bus from communicating over the bus includes the I/O device affecting the bus by the I/O device transmitting an undesired signal on the at least one data line of the bus, where the device processors severing of the communication link with the bus allows the other I/O devices to communicate to one another over the bus.

23. **(original)** The I/O device of claim 12 wherein the device processors fault detection includes the device processor attempting to affect the bus using the interface, wherein the device processor detects the potential device fault by an inability of the device processor to affect the bus.

24. **(original)** The I/O device of claim 23 wherein the device processor attempting to affect the bus includes the device processor attempting to change the state of the bus.

25. **(original)** The I/O device of claim 24 wherein the device processor attempting to change the state of the bus includes the device processor forcing a state on the bus.

26. **(original)** The I/O device of claim 25 wherein the device processor forcing the state of the bus includes the device processor transmitting one of a digital high value and a digital low value on the bus.

27. **(original)** The I/O device of claim 23 further comprising the device processor reading the bus after attempting to affect the bus, wherein the device processor determines the inability to affect the bus using the reading of the bus.

28. **(currently amended)** The I/O device of claim 12 further comprising the device processor performing further fault detection upon severing of the communication link, wherein when the device processor detects no device fault from the further fault detection, the device processor ~~reestablished~~ reestablishes the communication link with the bus.

29. **(original)** The I/O device of claim 12 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising the I/O device being assigned to one of the synchronous time slots, where the device processor performs fault detection during the asynchronous time slot following the corresponding synchronous time slot.

30. **(original)** The I/O device of claim 12 wherein the device processor performs the fault detection when the I/O device is not transmitting I/O device information on the bus.

31. **(original)** A field device for use in a process control system, the process control system including an I/O device and a plurality of field devices in communication with the I/O device using a bus segment, the field device comprising:

a field interface for communicatively linking the field device with the bus segment; and

a field device processor coupled with the field interface for controlling operation of the field device including performing fault detection for the field device;

wherein the field device processor, upon detection of a potential field device fault, severs the communication link provided by the field interface with the bus segment.

32. **(original)** The field device of claim 31 wherein the bus segment includes a data line and the field interface communicatively links the field device with the data line of the bus segment, and wherein the field device processor, upon detection of the potential field device fault, severs the communication link provided by the field interface with the data line.

33. **(original)** The field device of claim 32 wherein the field device further comprises a relay device coupled between the field device processor and the data line of the bus segment, the relay having a first state communicatively linking the field device with the data line, and a second state severing the communicative link between the field device and the data line of the bus segment, wherein the field device processor, upon detection of the potential field device fault, severs the communication link with the bus segment by actuating the relay to the second state.

34. **(original)** The field device of claim 32 wherein the data line of the bus segment is a data line capable of being affected by the field device.

35. **(original)** The field device of claim 31 wherein the field device processor fault detection includes the field device processor attempting to affect the bus segment using the interface, wherein the field device processor detects the potential field device fault by an inability of the field device processor to affect the bus.

36. **(currently amended)** The field device of claim 31 further comprising the field device processor performing further fault detection upon severing of the communication link, wherein when the field device processor detects no field device fault from the further fault detection, the field device processor ~~reestablished~~ reestablishes the communication link with the bus.

37. **(original)** A process control system for communications in a process control network having a plurality of devices in communication using a bus, the process control system comprising:

a primary redundant device communicatively linked to the bus; and

a secondary redundant device communicatively linked to the bus, and programmed to detect a primary redundant device fault;

wherein, the secondary redundant device, upon detecting the primary redundant device fault, publishes a primary redundant device fault message on the bus.

38. **(original)** The process control system of claim 37 further comprising a controller communicatively linked to the bus and including a controller processor programmed to process messages published on the bus, wherein the controller deactivates the primary redundant device responsive to the primary redundant device fault message.

39. **(original)** The process control system of claim 38 further comprising the controller activating the secondary redundant device.

40. **(original)** The process control system of claim 38 wherein the primary redundant device is further programmed to perform fault detection, and further comprising a primary fault detect order message published by the controller causing the primary redundant device to perform fault detection.

41. **(original)** The process control system of claim 40 wherein the secondary redundant device is capable of detecting secondary redundant device faults, and further comprising:

a primary redundant device no fault message published on the bus to the controller where no fault is detected in the primary redundant device; and

a secondary fault detect order message published by the controller responsive to the primary redundant device no fault message causing the secondary redundant device to perform fault detection.

42. **(original)** The process control system of claim 37 wherein the primary redundant device is further programmed to perform fault detection, and responsive to the primary redundant device fault message, the primary redundancy device performs fault detection.

43. **(original)** The process control system of claim 37 further comprising a direct communication link between the primary redundant device and the secondary redundant device, wherein the secondary redundant device detects the primary redundant device fault using the direct communication link.

44. **(original)** The process control system of claim 43 wherein the secondary redundant device detects the primary redundant device fault based on information received over the direct communication link.

45. **(original)** A method of configuring an input/output (I/O) device for use in a process control system, the process control system having a controller operating under a particular version of I/O communication software, the method comprising:

storing a plurality of versions of I/O communication software in a storage device for the I/O device, each version of I/O communication software usable by a device processor of the I/O device in controlling the I/O device;

determining by the device processor the particular version of I/O communication software utilized by the controller;

determining by the device processor a version of I/O communication software of the plurality of versions of I/O communication software stored in the storage device that is compatible with the particular version of communication protocol used by the controller; and

configuring the I/O device to operate using the compatible version of I/O communication software.

46. **(original)** The method of claim 45 wherein the controller transmits a message to the I/O device, and further comprising generating a responsive message at the device processor including information regarding the versions of I/O communication software stored in the storage device of the I/O device.

47. **(original)** The method of claim 46 wherein the version of I/O communication software comprises a plurality of versions including a primitive version and at least one less primitive version, and the generating a responsive message includes generating a first message portion utilized in the primitive version and the less primitive version of the I/O communication software, and generating a second portion utilized only in the less primitive version of the I/O communication software, and placing the information regarding the version of the I/O communication software stored in the storage device in the second message portion.

48. **(original)** The method of claim 47 wherein the message generated by the controller is a first message, and further comprising:

generating a second message by the controller including a first message portion utilized in the primitive version and the less primitive version of the I/O communication software, and a second portion utilized only in the less primitive version of the I/O communication software;

placing information by the controller in the second portion of the second message when the controller uses a less primitive version of the I/O communication software, and

leaving the second portion of the second message unused when the controller utilizes the primitive version of the I/O communication software;

sending the second message from the controller to the I/O device; and

determining by the device processor the particular version of I/O communication software utilized by the controller responsive to information placed in the second portion of the second message.

49. **(original)** The method of claim 45 further comprising:

generating an identification message at the controller including information regarding the version of I/O communication software utilized by the controller; and

sending the identification message from the controller to the I/O device;

wherein the determining of a version of I/O communication software includes extracting the version information from the identification message by the device processor, and determining the particular version of I/O communication software utilized by the controller using the version information.

50. **(original)** The method of claim 49 further comprising generating by the device processor a reply identification message responsive to the identification message identifying the versions of the I/O communication software stored in the storage device.

51. **(original)** The method of claim 45 wherein the determining of the compatible version of I/O communication software includes determining at the device processor the same version of I/O communication software as the particular version of I/O communication software utilized by the controller.

52. **(original)** The method of claim 45 wherein the determining of the compatible version of I/O communication software includes determining at the device processor a more primitive version of I/O communication software than the particular version of I/O communication software utilized by the controller.

53. **(original)** The method of claim 45 wherein the I/O device is communicatively linked to at least one field device, and further comprising communicating with the at least one field device using a Fieldbus communication protocol.

54. **(original)** The method of claim 45 wherein the I/O device is communicatively linked to at least one field device, and further comprising communicating with the at least one field device using a HART communication protocol.

55. **(original)** The method of claim 45 wherein the I/O device is communicatively linked to at least one field device, and further comprising communicating with the at least one field device using a 4-20 milliamp communication protocol.

56. **(original)** A method for severing communication between an input/output (I/O) device and a process control system, the process control system including a plurality of I/O devices communicatively linked using a bus, the method comprising:

providing an interface for communicatively linking the I/O device with the bus;

performing fault detection by a device processor of the I/O device; and

severing the communication link provided by the interface when the device processor detects a potential device fault in the I/O device.

57. **(original)** The method of claim 56 wherein the bus includes a data line, and:

providing the interface includes providing the interface for communicatively linking the I/O device with the data line; and

the severing of the communication link includes severing the communication link provided by the interface with the data line when the device processor detects a potential device fault in the I/O device.

58. **(original)** The method of claim 57 wherein the I/O device further comprises:

providing a relay device between the device processor and the interface, the relay communicatively linking the I/O device with the data line in a first state, and severing the communicative link between the I/O device and the data line of the bus in a second state;

wherein the severing of the communication link provided by the interface includes actuating the relay to the second state by the device processor.

59. **(original)** The method of claim 57 wherein the severing of the communication link provided by the interface with the data line includes severing the communication link provided by the interface with a data line capable of being affected by the I/O device.

60. **(original)** The method of claim 59 wherein the severing of the communication link provided by the interface with the data line includes severing the communication link provided by the interface with at least one of a transmit data line and clock data line.

61. **(original)** The method of claim 57 and further comprising:

providing a driver device between the device processor and the interface, the device driver having a driver output coupled to the interface and the device processor; and

performing further fault detection on the I/O device by forcing states to the driver output and reading the state of the driver output by the device processor upon severing the communication link with the interface;

wherein determining of the device fault includes determining of the device fault responsive to the reading of the state of the driver output.

62. **(original)** The method of claim 56 wherein the bus includes a plurality of data lines, and

providing the interface includes providing the interface communicatively linking the I/O device to the plurality of data lines,

wherein the severing of the communication link includes severing the communication link provided by the interface to the plurality of data lines of the bus upon detection of a device fault.

63. **(currently amended)** The method of claim 56 wherein the fault detection is an initial fault detection, and further comprising:

performing a later fault detection by the I/O device after the communicative link from the I/O device and the bus is severed.

64. **(original)** The method of claim 63 wherein the performing the later fault detection includes performing the later fault detection in a similar manner as the initial fault detection.

65. **(original)** The method of claim 63 further comprising reestablishing the communication link with the bus by the device processor when the later fault detection detects no I/O device fault.

66. **(original)** The method of claim 56 wherein the performing the fault detection includes attempting to affect the bus using the communicating link, wherein the potential device fault is detected by an inability to affect the bus.

67. **(original)** The method of claim 66 wherein the attempting to affect the bus includes attempting to change the state of the bus.

68. **(original)** The method of claim 67 wherein the attempting to change the state of the bus includes forcing a state on the bus.

69. **(original)** The method of claim 68 wherein the forcing the state of the bus includes forcing the bus to one of a digital high value and a digital low value.

70. **(original)** The method of claim 56 wherein the process control system operates in macrocycles, the macrocycles including at least one synchronous time slot and at least one asynchronous time slot corresponding to the synchronous time slot, and further comprising assigning the I/O device to one of the synchronous time slots, wherein the performing of the fault detection by the device processor includes performing the fault detection during the asynchronous time slot following the corresponding synchronous time slot which the I/O device is assigned.

71. **(original)** The method of claim 56 wherein the performing of the fault detection by the device processor includes performing the fault detection when the I/O device is not transmitting I/O device information on the bus.

72. **(currently amended)** A method for fault detection for an I/O device of a process control system having a plurality of I/O devices and a controller in ~~communicatin~~ communication using a bus, the method comprising:

providing a primary redundant device communicatively linked to the bus;

providing a secondary redundant device communicatively linked to the bus, and programmed to detect a primary redundant device fault;

detecting the primary redundant device fault by the secondary redundant device; and

publishing by the secondary redundant device a primary redundant device fault message on the bus.

73. **(original)** The method of claim 72 further comprising,

providing a controller device communicatively linked to the bus and including a controller processor programmed to process messages published on the bus containing the first unique address,

receiving the primary redundant device fault message at the controller, and

deactivating by the controller the primary redundant device responsive to the primary redundant device fault message.

74. **(original)** The method of claim 73 further comprising activating by the controller the secondary redundant device.

75. **(currently amended)** The method of claim 73 wherein the primary redundant device is further programmed to perform fault detection, and further comprising:

generating a primary fault detect order message by the controller ordering the primary redundant device to perform fault detection, and

publishing the primary fault detect order message on the bus by the controller to the primary redundant device.

76. **(original)** The method of claim 75 wherein the secondary redundant device is programmed to perform secondary redundant device fault detection, and further comprising:

generating a primary redundant device no fault message at the primary redundant device where no fault is detected in the primary redundant device;

publishing the primary redundant device no fault message on the bus to the controller;

generating at the controller a secondary fault detect order message responsive to the primary redundant device no fault message ordering the secondary redundant device to perform fault detection; and

publishing by the controller the secondary fault detect order message on the bus to the secondary redundant device.

77. **(original)** The method of claim 72 wherein the primary redundant device is further programmed to perform fault detection, and further comprising performing fault detection at the primary redundant device responsive to the publishing of the primary redundant device fault message.

78. **(original)** The method of claim 72 further comprising providing a direct communication link between the primary redundant device and the secondary redundant device, wherein the detecting of the primary redundant device fault by the secondary redundant device includes detecting the primary redundant device fault using the direct communication link.

79. **(original)** The method of claim 78 wherein the detecting of the primary redundant device fault includes detecting the primary redundant device fault based on information received over the direct communication link.

80. **(new)** An apparatus for use in a process control system, the process control system including a plurality of devices in communication using a bus, the apparatus comprising:

an interface for communicatively linking the apparatus with the bus;

a processor coupled with the interface for controlling operation of the apparatus including performing fault detection for the apparatus;

wherein the processor, upon detection of a potential apparatus fault, severs the communication link provided by the interface with the bus.

81. **(new)** The apparatus of claim 80 wherein the apparatus is a field device.

82. **(new)** The apparatus of claim 81 wherein the bus includes a data line and the interface communicatively links the apparatus with the data line of the bus, and wherein the processor, upon detection of the potential apparatus fault, severs the communication link provided by the interface with the data line.

83. **(new)** The apparatus of claim 82 wherein the apparatus further comprises a relay coupled between the processor and the data line of the bus, the relay having a first state communicatively linking the apparatus with the data line, and a second state severing the communicative link between the apparatus and the data line of the bus, wherein the processor, upon detection of the potential apparatus fault, severs the communication link with the bus by actuating the relay to the second state.

84. **(new)** The apparatus of claim 82 wherein the data line of the bus is a data line capable of being affected by the apparatus.

85. **(new)** The apparatus of claim 81 wherein the processor fault detection includes the processor attempting to affect the bus using the interface, wherein the processor detects the potential apparatus fault by an inability of the processor to affect the bus.

86. **(new)** The apparatus of claim 81 further comprising the processor performing further fault detection upon severing of the communication link, wherein when the processor detects no apparatus fault from the further fault detection, the processor reestablishes the communication link with the bus.

87. **(new)** The apparatus of claim 80 wherein the apparatus is an input/output (I/O) device.

88. **(new)** The apparatus of claim 87 wherein the bus includes a data line and the interface communicatively links the apparatus with the data line of the bus, and wherein the processor, upon detection of the potential apparatus fault, severs the communication link provided by the interface with the data line.

89. **(new)** The apparatus of claim 88 wherein the apparatus further comprises a relay coupled between the processor and the data line of the bus, the relay having a first state communicatively linking the apparatus with the data line, and a second state severing the communicative link between the apparatus and the data line of the bus, wherein the processor, upon detection of the potential apparatus fault, severs the communication link with the bus by actuating the relay to the second state.

90. **(new)** The apparatus of claim 88 wherein the data line of the bus is a data line capable of being affected by the apparatus.